THERMAL SOLUTIONS FOR CHIP PACKAGING

Graphene Thermal Pad / Plate

SiP · 2.5D/3D heterogeneous integration · Chiplet · FCBGA · power modules

Pad 180 W/m·K Plate 1200 W/m·K (through-thickness)

180 W/m·K	<0.05 °C·cm²/W	≤10% drift	>5 kV/mm
Pad, through-thickness k	Thermal resistance @50 psi	150 °C × 1500 h aging	Dielectric strength

Four packaging pain points — solved one by one

1 · Warpage / poor coplanarity → uneven BLT, hot spots

High compression and rebound: conforms from 10–50 psi; choose 0.3 / 0.5 / 0.7 mm to match warpage and even out the bond line.

2 · Grease pump-out, dry-out, contamination

Solid, no liquid vehicle: after 150 °C × 1500 h, resistance drift ≤10% and compression drift ≤10% (50 psi).

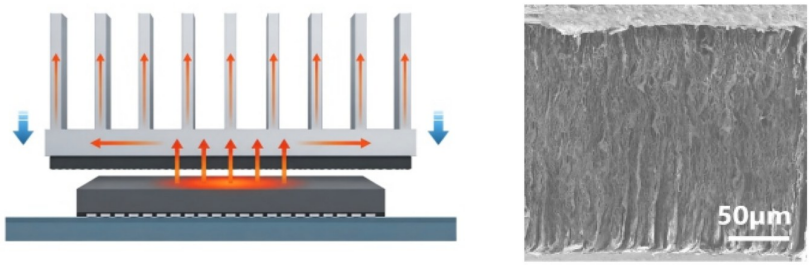
3 · Ordinary silicone pads conduct only 1–5 W/m·K

180 W/m·K through-thickness — over 30× an ordinary pad of the same thickness, directly lowering junction temperature.

4 · Anisotropic material used in the wrong direction

Vertically oriented structure: the high-conductivity axis is through the thickness (Z) — exactly die → lid / heatsink heat flow.

Why it works: heat path and microstructure



Left: heat path (die → thermal pad → spreader / heatsink). Right: SEM cross-section — vertically oriented graphene walls form a continuous through-thickness conduction channel (50 μm scale).

Compared with existing interface solutions

Dimension	Thermal grease	Ordinary silicone pad	Premium imported pad	Lenecold graphene pad
Through-thickness k (W/m·K)	—	1–5	15–25	**180**
Resistance @50 psi	Low, poor life	High	Medium	**<0.05 °C·cm²/W**
Pump-out / dry-out	Yes	Slight	Slight	**Solid — none**
150 °C × 1500 h	Clearly degrades	Permanent set	Moderate	**Resistance / compression ≤10%**
Dielectric strength	—	3–6 kV/mm	3–6 kV/mm	**>5 kV/mm**

Anonymised case: a 700 W-class AI accelerator package with EN-PAD-050 (0.5 mm) on a vapour chamber held the interface ΔT below 5 °C at 50 psi, sustaining full boost clocks.

Performance, selection and supply

Through-thickness graphene thermal solutions for chip packaging and power modules — data from material-level testing and aging validation

Key properties

Property	Pad EN-PAD series	Plate EN-PLT series
Conductivity	180 W/m·K (through-thickness)	1200 W/m·K (through-thickness)
Thermal resistance	<0.05 °C·cm²/W @ 50 psi	—
Density / CTE	—	1.5–4 g/cm³; CTE 4–12 ppm/K
Thickness	0.3 / 0.5 / 0.7 mm (custom 0.2–2.0)	0.5–3 mm
Operating temperature	−40 to +200 °C	−40 to +200 °C
Dielectric / processing	Breakdown >5 kV/mm; die-cut to ±0.05 mm	Insulating layer available; cut / drill / laminate

Reliability

Item	Condition	Result
High-temperature aging	150 °C × 1500 h	Resistance drift ≤10%, compression drift ≤10%
Interface stability	Power / thermal cycling	Solid — no pump-out, no dry-out, no migration
Dielectric / vacuum	Breakdown; TML-CVCM	Breakdown >5 kV/mm; outgassing reports on request

Package selection guide

Package scenario	Recommended stack	Note
FCBGA / large die (≥500 W)	EN-PAD-050 + vapour chamber	Thin BLT, low resistance
SiP / multi-die heterogeneous	EN-PAD-050 / 070	Absorbs coplanarity variation
2.5D / 3D stack (incl. HBM)	EN-PAD-030 / 050 + EN-PLT	Low stress, warp resistant
IGBT / SiC power module	EN-PAD-100 + EN-PLT-100 / 200	Power-cycling proven
Automotive / industrial	EN-PAD-100 / 150	Large gap, long life

Supply and engineering support

Standard sample
30 × 30 mm (0.5 mm thick)
From 1 piece, die-cut to drawing

Lead time
Sample in ~2 weeks
Production 2–3 weeks

Documents
Batch CoA, dimensional report
Resistance-vs-pressure, aging, TML-CVCM

Selection support
Send warpage, BLT, pressure, power and lifetime — we return a resistance budget and thickness

Indicative pricing (published; final quote by drawing and volume)
Thermal pad (30 × 30 mm, 0.5 mm): 1–5 pcs ¥80–150/pc | 10–100 pcs ¥50–80/pc | ≥1000 pcs ¥25–45/pc
Thermal plate: 1–3 pcs ¥800–1500/pc | 10–50 pcs ¥500–1000/pc | ≥500 pcs ¥300–600/pc

Qualification
ISO 9001 · CE · RoHS · REACH · UL94 V-0 · 18 related patents · Incubated by NGIC (National Graphene Innovation Center)

1. Send conditions → 2. Stack + resistance budget → 3. Samples in ~2 weeks

Send your package structure today — verifiable samples in 2 weeks

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